REMARKS

The Office Action dated November 20, 2003, has been received and carefully noted. The above amendments to the specification, figures, and claims, and the following remarks, are submitted as a full and complete response thereto. Claims 1, 3, 4, 6, 8 and 12 have been amended and claim 5 has been cancelled. Applicants respectfully assert that no new matter has been added through the above amendments. Claims 1-4 and 6-20 are again submitted for consideration.

In the Office Action, the specification, drawings and claim 6 were objected to because of minor errors. Applicants have amended the specification, added a replacement sheet providing a revised Fig. 8, and corrected the minor misspelling in claim 6, while placing that claim in independent form. Also, per the Examiner's suggestion, Applicants have examined the rest of the specification to correct additional errors in the specification than those indicated by the Examiner. Reconsideration and withdrawal of the objections are respectfully requested.

Claims 3, 4, 7 and 12-20 were rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. Claim 3 was alleged to be indefinite, first, because "it is unclear what receives the released memory address in the first clock cycle." Applicants respectfully traverse this portion of the rejection. Claim 3 is clear in that the claim is directed to a method for managing memory in a network switch and it is sufficient to define the method as occurring in the network switch. As an example, Applicants point to claim 1, wherein that claim does not explicitly recite "what" does the reading and the

writing steps, but claim 1 is clearly a method that is carried out with respect to a network switch. Similarly, Applicants respectfully assert that claim 3 is clear and particularly points out and distinctly claims the subject matter of the method recited therein.

With respect to the second portion of the rejection of claim 3, it is alleged that it is unclear that the second clock cycle is the next clock cycle after the first clock cycle. While the suggested language, recited in the rejection, for the claim is appreciated, Applicants note that the use of the limitation "the next clock cycle" would give rise to a new rejection under §112 for failing to have a proper antecedent basis. Applicants have amended claim 3 to address the point made in that portion of the rejection and Applicants respectfully assert that claim 3 is now definite under 35 U.S.C. §112, second paragraph.

Claim 4 was also rejected under 35 U.S.C. §112, second paragraph, because it was alleged that it was not clear what the memory address pointer is associated with. Applicants have amended claim 4 to reflect that the memory address pointer is associated with the memory of the network switch. Reconsideration and withdrawal of the rejection of claim 4 are respectfully requested.

Claim 7 was also rejected as being indefinite because "an address can be said to be in a stack only if the pointer is incremented or decremented" and it is alleged that claim 7 recited both writing to the stack and not moving the pointer. However, claim 6 recites only "an address released back to the stack" and NOT "written to the stack. As explained in the specification, at page 80, line 19 to page 81, line 10, this passing off of the address occurs when an address is released but before the released address is written into the pool

and saves clock cycles that would otherwise be used for the write and read operations. As such, Applicants respectfully assert that claim 7 is definite under 35 U.S.C. §112, second paragraph.

A similar assumption was also made in the rejection of claim 12. Therein it was alleged that claim 12 contradicts the features of claim 11. Applicants have amended claim 12 such that the claim comports with the subject matter recited in claims 7. As discussed above with respect to claim 7, Applicants respectfully assert that claim 12 is definite under 35 U.S.C. §112, second paragraph, and reconsideration and withdrawal are respectfully requested.

With respect to the rejection of claim 13, this portion of the rejection is traversed similarly to that of claim 3. In claim 13, it is clear in that the claim is directed to an apparatus for managing memory in a network switch and it is sufficient to define a request made for available memory addresses, where it is understood that the request is made to the apparatus, specifically the memory controller, as recited in the claim. Since claim 13 is directed only to an apparatus for managing memory, the further recitation of other elements of the network switch, such as those that would make the request, need not be recited. Applicants respectfully assert that claim 13 is clear and particularly points out and distinctly claims the subject matter of the apparatus recited therein.

With respect to the rejection of claim 20, this portion of the rejection is also traversed similarly to the rejection of claims 3 and 13. The rejection again indicates that it is unclear what requests an available memory address, releases a memory address and

when the address is passed off. As discussed above, it is not necessary for the claim to recite what makes a request as those limitations of the claim may be met by an apparatus for managing memory that is capable of receiving requests. Applicants respectfully assert that claim 20 is clear in that it recites that the reading and writing means are configured to pass off the address during certain circumstances. Applicants respectfully assert that claim 20 is clear and particularly points out and distinctly claims the subject matter of the apparatus recited therein. Reconsideration and withdrawal of the rejections of the claims under 5 U.S.C. §112, second paragraph, are respectfully requested.

Claims 1, 2, 5 and 8-11 were rejected under 35 U.S.C. §102(b) as being anticipated by *Heddes et al.* (U.S. Patent no. 5,432,908). Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Heddes et al.* in view of *Hine* (U.S. Patent no. 5,652,864). The above rejections, as might be applied against the present claims, are respectfully traversed according to the remarks that follow.

The present invention is directed, according to claim 1, to a method for managing memory in a network switch. The method includes providing a memory, wherein the memory includes a plurality of memory locations configured to store data therein, providing a memory address pool having a plurality of available memory addresses arranged therein, wherein each of the plurality of memory addresses corresponds to a specific memory location and providing a memory address pointer, wherein the memory address pointer indicates a next available memory address in the memory address pool. The method also includes reading available memory addresses from the memory address

pool using a last in first out operation, writing released memory addresses into the memory address pool and adjusting a position of the memory address pointer upon a read or a write operation from the memory address pool. The reading, writing and adjusting steps may include passing off the released memory addresses for the available memory addresses when a release of a released memory address occurs in a same clock cycle as a request for an available address.

The present invention is directed, according to claim 6, a method for managing memory. The method includes providing a memory having a predetermined number of memory storage locations therein providing a predetermined number of addresses in a stack, each of the predetermined number of addresses corresponding to a unique memory storage location and providing an address pointer for indicating a next available address to be used from the predetermined number of addresses in the stack, wherein the address pointer releases an address in a last-in first-out type operation. The method further includes the step of passing off an address released back to the stack to a request for an available address when a release of an address back to the stack occurs in the same clock cycle as the request for an available address.

The present invention is directed, according to claim 8, an apparatus for managing memory in a network switch. The apparatus includes a memory address pool having a plurality of memory addresses, each of the plurality of memory addresses corresponding to an individual memory location in a memory and a memory controller in connection with the memory and the memory address pool. The memory controller manages an

address pointer for indicating a next available memory address in the memory address pool and is configured to pass off the released memory address upon a request for the available memory address in the same clock cycle.

Common to the three independent claims discussed above, which were rejected over prior art, is that the control of the memory can include the step of passing off the released memory address upon a request for the available memory address in the same clock cycle. This process is discussed in the instant specification at page 80, line 18 to page 81, line 10 and allows for the elimination of multiple clock cycles from the operation. Neither reference cited in the Office Action, taken alone or together, teaches or suggests at least this element of the independent claims.

Heddes et al. is directed to a system for management of high speed buffers of shared memory using linked lists and buffer managers. The buffers are part of a larger memory and are managed by a buffer manager. The manager provides a pointer, where data is stored in a linked list fashion. The anticipation rejection of claim 1 notes that incrementing or decrementing a pointer for a stack when an element is added or subtracted therefrom is "*well known in the art*," and appears to acknowledge that the element is not disclosed in *Heddes et al.* Because of this, Applicants respectfully assert that the rejection of at least claim 1 is improper on its face because the rejection acknowledges that *Heddes et al.* fails to teach all of the elements of that claim.

With respect to the rejection of claim 6, the Office Action acknowledges the deficiencies of *Heddes et al.* and thus also cites *Hine*. The Office Action, apparently,

acknowledges that *Heddes et al.* fails to disclose the passing off of a released address and alleges that *Hine* discloses the missing element. *Hine* is directed to the concurrent storage allocations or returns without need to lock free storage chain. The reference is concerned with the fragmentation in memory that occurs when memory blocks of various sizes are allocated and returned.

However, even if Applicants accepted the contentions raised in the rejections, i.e that *Hine* discloses the concurrent allocation and storage of blocks and thus the request and release of memory occur within the same clock cycle, that is not the same as the passing off of an address released in response to a request that occurs in the same clock cycle. The independent claims subject to prior art rejections, namely claims 1, 6 and 8, recite, in part, that the memory controller is configured to pass off the released memory address upon a request for the available memory address in the same clock cycle. Neither *Heddes et al.* nor *Hine* teaches or suggests this element of those independent claims.

Put another way, the concurrent allocation and storage in memory is not the same as substituting a just released memory to fulfill a just received request for memory. At most, the references taken together could possibly teach a linked list memory system where allocation and return of memory block sections of the memory can occur concurrently. As asserted above, that is not the same as passing off a released memory address upon a request for an available memory address in the same clock cycle. Applicants respectfully assert that *Heddes et al.* and *Hine* fail to teach or suggest all of

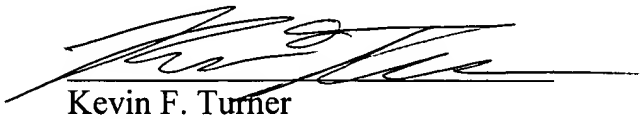
the elements of claims 1, 6 and 8 and the rejection must therefore be held to be improper. Reconsideration and withdrawal of the rejections are respectfully requested.

In a similar fashion, Applicants respectfully assert that claims 2, 7 and 9-12 should be allowed for at least their dependence on claims 1, 6 and 8. Applicants also note that while independent claims 3, 13 and 20 were not rejected over prior art, all three independent claims contain subject matter similar to that discussed above with respect to claims 1, 6 and 8. As such, Applicants respectfully request allowance of claims 3, 13 and 20, as well as claims 4 and 14-19 dependent thereon, and request that the application be allowed to proceed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Kevin F. Turner
Registration No. 43,437

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

KFT:lls